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LAHIVE & COCKFIELD, LLP. 28 STATE STREET BOSTON, MA 02109			STEVENS, THOMAS H	
			ART UNIT	PAPER NUMBER
			2123	
DATE MAILED: 04/28/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/870,280

Applicant(s)

SHAKERI ET AL.

Examiner

Thomas H. Stevens

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 10 January 2005.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-36 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

1. Claims 1-36.

### ***Section I: Response to Applicant's Arguments***

#### ***35 USC § 103***

2. Applicants are thanked for addressing this issue. Applicants' response focuses on the prior art does not teach, verbatim, nor *suggest generating or grouping a plurality of output signals values as an ordered set in a multiplexer as a first composite signal.*

The examiner points specifically to applicants' specification on page 4, paragraphs 3 and 4 that discloses, "composite signals simplify the generation of block diagram in a visual appearance, to which Paradis (pg. 5, left column 3<sup>rd</sup> paragraph, figure2 [complex system]) teaches. Additionally, applicants' stated none of the cited prior art suggests a plurality of output signals as an ordered set in a multiplexer as a first composite signal, when in fact, System View on pages 163 and 167 teaches, complex block and multiplex block, respectively; with a logic threshold block to handle two outputs (pg. 179).

Furthermore, System View<sup>®</sup> graphically teaches two signals (I and Q channel of a M-ary PSK (Phase shift keying)) in the time domain with their composite coupled to noise (pg. 273).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the

How does this respond to the arguments here

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references themselves or in the knowledge generally available to one of ordinary skill in the art. Rejection stands.

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Section II: Rejections (Final Rejection 2<sup>nd</sup> Office Action)

***Claim Rejections - 35 USC § 103***

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable by Paredis et al., in view of System View<sup>®</sup> (Elanix Incorporated (1994-1999)). System View teaches a dynamic analysis engineering/scientific design simulation in real-time; however this software program doesn't teach a hierarchy of functional blocks with Internet access. Paredis et al., ("Composable Models for Simulation-based Design" (2000)). Paredis et al., teaches the concept of combining both form (CAD models) and behavior (simulation models) of mechatronic system components into component objects (abstract) in a "tree structure" which Internet accessible.

At the time the invention, it would have been obvious to one of ordinary skill in the art to use Paredis et al., to modify Elanix's System View<sup>®</sup> to maintain consistency between the form and the behavior of the component objects with the assistance of Internet-based active languages such as Java and C++ (Paredis: abstract, 3<sup>rd</sup> and 4<sup>th</sup> paragraphs respectively)

Claim 1. A modeling process comprising: providing a plurality of blocks, each of the blocks representing functional entities (Paredis: pg. 2 and 3, Simulation Integrated with CAD); generating a plurality of output signal values from the plurality of blocks (Elanix: pgs. 35-36, section 4.9); grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal (Paredis: pg. 5, left column, lines 4-8); and outputting the first composite signal (Paredis: pg. 5, left/right columns, lines 20-25 and 1-13, respectively).

Claim 2. The process of claim 1 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; Elanix: pgs. 35-36, section 4.9) wherein each of the blocks includes at least one output signal port (Elanix: pgs. 35-36, section 4.9).

Claim 3. The process of claim 1 (Paredis: pg. 2 and 3, Simulation Integrated with CAD;

Elanix: pgs. 35-36, section 4.9) wherein a plurality of input signal values and the output signal values have at least one attribute (Elanix: pgs 17-18, section 3.3.7).

Claim 4. The process of claim 3 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; Elanix: pgs. 35-36, section 4.9), wherein the attribute is a name (Elanix: pgs 17-18, section 3.3.7).

Claim 5. The process of claim 3, (Paredis: pg. 2 and 3, Simulation Integrated with CAD; Elanix: pgs. 35-36, section 4.9) wherein the attribute is a data type (Paredis: pg. 7, right column, lines 11-16 and figure 5).

Claim 6. The process of claim 3 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; Elanix: pgs. 35-36, section 4.9) wherein the attribute is numeric type (Paredis: pg. 8, right column, lines 11-26).

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Claim 7. The process of claim 3, (Paredis: pg. 2 and 3, Simulation Integrated with CAD) wherein the attribute is a dimensionality (Paredis: pg 6-7, right column, last paragraph and left column first paragraph, respectively with figure 4).

Claim 8. The process of claim 1 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; Elanix: pgs. 35-36, section 4.9) wherein the ordered set is a linked list data structure (Paredis: pg 6-7, right column, last paragraph and left column first paragraph, respectively with figure 4).

Claim 9. The process of claim 8 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; Elanix: pgs. 35-36, section 4.9) wherein the linked list data structure is a tree data structure, the tree data structure including  $m + n$  nodes (Paredis: pg 6-7, right column, last paragraph and left column first paragraph, respectively with figure 4; and pg. 6, left column, lines 13-36 with figure 3).

Claim 10. The process of claim 9 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; Elanix: pgs. 35-36, section 4.9), (Paredis: pg 6-7, right column, last paragraph and left column first paragraph, respectively with figure 4; and pg. 6, left column, lines 13-36 with figure 3) wherein  $m$  represents a number of independent signals and  $n$  represents a number of composite signals.

Claim 11. The process of claim 1 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; Elanix: pgs. 35-36, section 4.9) further comprising decomposing the first composite signal into the plurality of output signals in a demultiplexer.

Claim 12. The process of claim 1 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; Elanix: pgs. 35-36, section 4.9) further comprising viewing the ordered set contained in the first composite signal with a composite signal viewer (Elanix: pgs 272-273 with pg. 101, figure 7.5).

Claim 13. The process of claim 1 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; Elanix: pgs. 35-36, section 4.9) wherein at least one of the input signal values is a second composite signal (Elanix: pgs 272-273).

Claim 14. A block diagram modeling process comprising: providing a first block and a second block, the blocks representing functional entities (Paredis: pg. 2 and 3, Simulation Integrated with CAD; and Elanix: pgs. 23-25, 3.4 example); generating a plurality of output signal values from the first and second block (Elanix: pgs 272-273); grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal (Elanix: pgs 272-273); and processing the composite signal in a third block (Elanix: pgs 272-273).



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Claim 15. The process of claim 14 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; and Elanix: pgs. 23-25, 3.4 example) wherein the ordered set is a linked list data structure (Paredis: pg 6-7, right column, last paragraph and left column first paragraph, respectively with figure 4).

Claim 16. The process of claim 14 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; and Elanix: pgs. 23-25, 3.4 example) wherein an input signal is a second composite signal (Elanix: pg 209).

Claim 17. The process of claim 14 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; and Elanix: pgs. 23-25, 3.4 example) further comprising decomposing the composite signal into a plurality of input signal values (Elanix: pgs 272-273, specifically figure E.7-1 the output of block 7 is now the inputs of 1 and 2, the in-phase and quadrature signals, respectively).

Claim 18. The process of claim 14, (Paredis: pg. 2 and 3, Simulation Integrated with CAD; and Elanix: pgs. 23-25, 3.4 example) wherein at least one of the input signals is a second composite signal (Elanix: pgs 272-273, specifically figure E.7-1 the output of block 7 is now the inputs of 1 and 2, the in-phase and quadrature signals, respectively).

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Claim 19. The process of claim 18 (Paredis: pg. 2 and 3, Simulation Integrated with CAD; and Elanix: pgs. 23-25, 3.4 example) wherein the composite signal viewer displays the ordered set contained in the composite signal on a graphical user interface (GUI) (Paredis: pg. right column 3<sup>rd</sup> paragraph with figures 9 and 10).

Claim 20. The process of claim 19, (Paredis: pg. 2 and 3, Simulation Integrated with CAD; and Elanix: pgs. 23-25, 3.4 example) wherein the GUI is provided on an input/output device (Paredis: pg. 10 right column 3<sup>rd</sup> paragraph with figures 9 and 10 and Elanix: pg. 12, section 2.0).

Claim 21. A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to (Paredis: pg. 2 and 3, Simulation Integrated with CAD, 10 right column 3<sup>rd</sup> paragraph with figures 9 and 10; and Elanix: pgs. 23-25, section 3.4 example, pg. 12, section 2.0): provide a plurality of blocks, each of the blocks representing functional entities; generate a plurality of output signal values from the plurality of blocks (Elanix: pg. 24); group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal (Elanix: pgs 272-273, specifically figure E.7-1 block 10); and output the first composite signal (Elanix: pgs 272-273, specifically figure E.7-1 block 7).

Claim 22. The computer program product of claim 21 (Paredis: pg. 2 and 3, Simulation Integrated with CAD, 10 right column 3<sup>rd</sup> paragraph with figures 9 and

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10; and Elanix: pgs. 23-25, section 3.4 example, pg.12, section 2.0) wherein the computer readable medium is a random access memory (RAM) (Elanix: pgs pg.12, section 2.0).

Claim 23. The computer program of claim 21(Paredis: pg. 2 and 3,Simulation Integrated with CAD, 10 right column 3<sup>rd</sup> paragraph with figures 9 and 10; and Elanix: pgs. 23-25, 3.4 example, pg.12, section 2.0) wherein the computer readable medium is read only memory (ROM).

Claim 24. The computer program of claim 21 (Paredis: pg. 2 and 3,Simulation Integrated with CAD, 10 right column 3<sup>rd</sup> paragraph with figures 9 and 10; and Elanix: pgs. 23-25, section 3.4 example, pg.12, section 2.0) wherein the computer readable medium is hard disk drive.

Claim 25. A processor and a memory configured to: provide a plurality of blocks, each of the blocks representing functional entities; generate a plurality of output signal values from the plurality of blocks (Paredis: pg. 2 and 3,Simulation Integrated with CAD, 10 right column 3<sup>rd</sup> paragraph with figures 9 and 10; and Elanix: pgs. 23-25, 3.4 example, pg.12, section 2.0); group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal (Elanix: pgs 272-273, specifically figure E.7-1 the output of block 7 is now the inputs of 1 and 2, the in-phase and quadrature signals, respectively); and output the first composite signal

(Elanix: pgs 272-273, specifically figure E.7-1 the output of block 7 is now the inputs of 1 and 2, the in-phase and quadrature signals, respectively).

Claim 26. The processor and memory of claim 25 (Paredis: pg. 2 and 3, Simulation Integrated with CAD, 10 right column 3<sup>rd</sup> paragraph with figures 9 and 10; and Elanix: pgs. 23-25, section 3.4 example, pg.12, section 2.0) wherein the processor and the memory are incorporated into a personal computer.

Claim 27. The processor and memory of claim 25 (Paredis: pg. 2 and 3, Simulation Integrated with CAD, 10 right column 3<sup>rd</sup> paragraph with figures 9 and 10; and Elanix: pgs. 23-25, section 3.4 example, pg.12, section 2.0) wherein the processor and the memory are incorporated into a network server residing in the Internet (Paredis: pg. 9, right column, lines 32-36).

Claim 28. The processor and memory of claim 25 (Paredis: pg. 2 and 3, Simulation Integrated with CAD, 10 right column 3<sup>rd</sup> paragraph with figures 9 and 10; and Elanix: pgs. 23-25, section 3.4 example, pg.12, section 2.0) wherein the processor and the memory are incorporated into a single board computer.

Claim 29. A modeling process comprising: providing a plurality of blocks, each of the blocks representing a functional entity that generates one or more output signals (Paredis: pg 6-7, right column, last paragraph and left column first paragraph,

respectively with figure 4;and Elanix: pgs. 23-25, section 3.4 example); grouping the output signals as an ordered set in a multiplexer as a composite signal (Elanix: pgs 272-273, specifically figure E.7-1 the output of block 7 is now the inputs of 1 and 2, the in-phase and quadrature signals, respectively); and outputting the composite signal(Elanix: pgs 272-273, specifically figure E.7-1 the output of block 7 is now the inputs of 1 and 2, the in-phase and quadrature signals, respectively).

Claim 30. The process of claim 29 (Paredis: pg 6-7, right column, last paragraph and left column first paragraph, respectively with figure 4;and Elanix: pgs. 23-25, section 3.4 example) wherein the ordered set is a tree data structure.

Claim 31. The process of claim 30 (Paredis: pg 6-7, right column, last paragraph and left column first paragraph, respectively with figure 4;and Elanix: pgs. 23-25, section 3.4 example) wherein the tree data structure is a linked list.

Claim 32. The process of claim 29 (Paredis: pg 6-7, right column, last paragraph and left column first paragraph, respectively with figure 4;and Elanix: pgs. 23-25, section 3.4 example) further comprising: providing a composite signal viewer (Elanix: pg 209); and viewing the ordered set in a graphical user interface executing in the composite signal viewer (Elanix: pg 209).

Claim 33. A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to (Paredis: pg 6-7, right column, last paragraph and left column first paragraph, respectively with figure 4; and Elanix: pgs. 23-25, section 3.4 example with pg 209): provide a plurality of blocks, each of the blocks representing a functional entity that generates one or more output signal values; group the output signals as an ordered set in a multiplexer as a composite signal; and output the composite signal (Elanix: pgs 272-273 and pg. 209).

Claim 34. A processor and memory configured to provide a plurality of blocks, each of the blocks representing a functional entity that generates one or more output signal values (Paredis: pg 6-7, right column, last paragraph and left column first paragraph, respectively with figure 4; and Elanix: pgs. 23-25, section 3.4 example with pg. 209 and pgs. 272-273); group the output signals as an ordered set in a multiplexer as a composite signal (Elanix: pgs 272-273, specifically figure E.7-1 the output of block 7 is now the inputs of 1 and 2, the in-phase and quadrature signals, respectively); and output the composite signal (Elanix: pgs 272-273, specifically figure E.7-1 the output of block 7 is now the inputs of 1 and 2, the in-phase and quadrature signals, respectively).

Claim 35. A method for providing a composite signal in a modeling signal (Paradis: abstract and title with pg. 5, left column, 3<sup>rd</sup> paragraph, 3 sentence) in a modeling environment, the method comprising the steps of: providing a plurality of output

signals from one or more blocks: generating a composite signal comprising a set of the plurality of output signals; and providing the composite signal as an output signal (System View<sup>®</sup>: M-ary PSK's I and Q channel relationship (pg. 273);

Claim 36. A method for graphically representing a composite signal in a modeling environment, the method comprising the steps of: providing a plurality of output signals from one or more blocks, each output signal graphically indicated by a signal identifier; and providing a composite signal identifier representing a composite signal (System View<sup>®</sup>: M-ary PSK's I and Q channel relationship (pg. 273) comprising a set of the plurality of output signals.

### ***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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***Correspondence Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Kevin Teska at (571) 272-3716. Fax number is 571-273-3715.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

April 19, 2005

THS

  
KEVIN J. TESKA  
SUPERVISORY  
PATENT EXAMINER